IDEC Chip Design Contest



A Reconfigurable Ultrasonic Pulser-Reciever Circuit for a **Transducer with Large Capacitive Load**

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Introduction

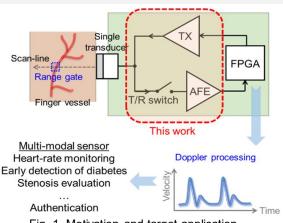


Fig. 1. Motivation and target application

- Target application
- Ultrasonic sensor module with single transducer
- Focus of this work
- Transducer interface circuit with reconfigurable topology
- Primary requirements and countermeasures

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Requirement	Countermeasure	
Large capacitive load (few nF) Center freq. up to 10 MHz	Minimum transistor stack in High-voltage pulser	
Small active area	Reconfigurable topology including pulse and T/R switch	
Low noise performance of preamplifier	Optimization of operational region of transistors	

Schematic Diagram

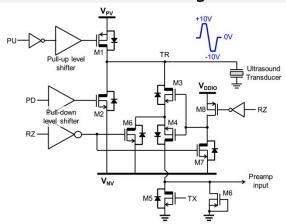


Fig. 2. Schematic of high-voltage pulser with T/R switch

- Reconfigurable high-voltage pulser with T/R switch
- Bipolar/Unipolar pulsing with 5V/3.3V logic control
- GND-path HV switch reconfigured as T/R switch

Measurements

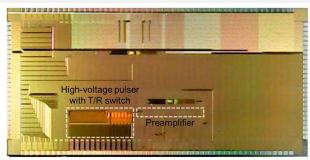


Fig. 3. Chip micrograph



Fig. 4. Measured waveforms

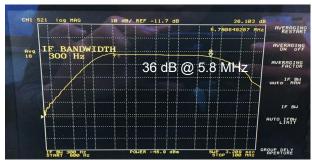


Fig. 5. Measured frequency response of preamplifier

Summary

	This work	JSSC'20	JSSC'13
Process	180nm BCD	180nm BCD	180nm HV CMOS
Max output	20 Vpp	60 Vpp	30 Vpp
Max. carrier frequency	11 MHz	9 MHz	3.3 MHz
Load cap	5 nF	18 pF	40 pF
T/R embedded	Yes	Yes	No
Active area	0.31 mm ²	0.167 mm ²	0.33 mm^2

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